Ordering number : EN2169C

CMOS LSI



LC7537, 7537AN, 7537NE

Electronic Volume Control System for Audio Equipment

Overview

The LC7537N is an electronic control LSI capable of electronically controlling the volume, balance, loudness, fader, bass, and treble functions individually with fewer externally connected component parts.

Features

- Enables controlling the below-listed functions with 3-line serial data, including CE, DI, and CLK. Also, due to 0 V to 5 V swing of the serial data input voltage, permits the use of a general purpose microcomputer.

  Volume : Separately controls the Lch and Rch volume levels across 81 positions over the 0 dB to –79 dB (in 1 dB steps) range and –∞, and consequently also serves balance control purposes.

  Loudness : By virtue of a center tap provided at the –20 dB position of the volume controlling ladder resistors, permits loudness to be controlled with externally connected CR components.

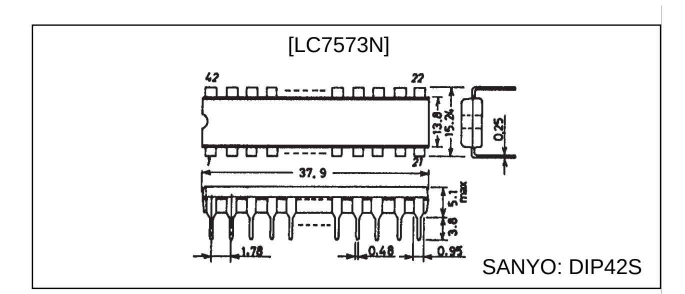
  Fader : By varying only the rear or front output level across 16 positions, provides fader functions (in 2 dB steps over the 0 dB to –20 dB range, and 5 dB steps over the –20 dB to –45 dB range, and at –∞, for a total of 16 positions).

  Bass/Treble : With CR components externally connected, forms an NF type tone control circuit (Baxandall type) to exercise control across 15 positions over both the bass and treble functions in 2 dB steps.
- By virtue of its CMOS structure, the LSI operates under a broad power supply voltage range from +4.5 V to +15 V, permitting the use of either a single or a dual ± power supply, whichever is preferred.

Package Dimensions

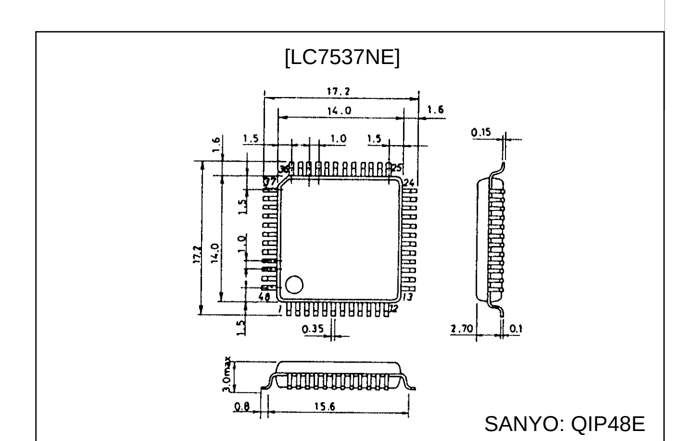
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3025B-DIP42S



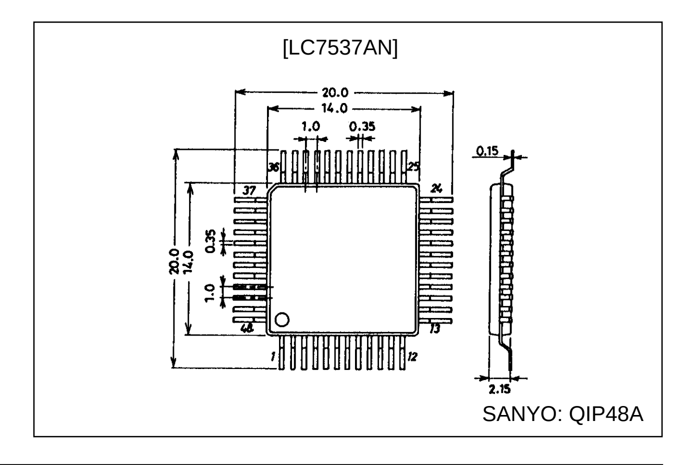
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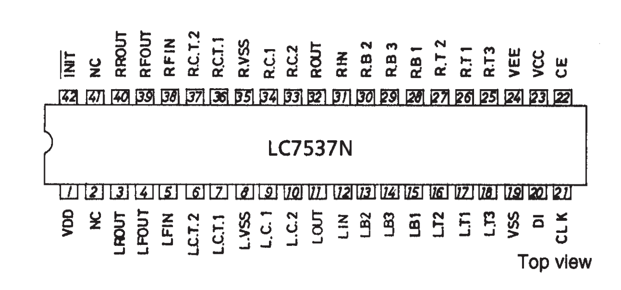


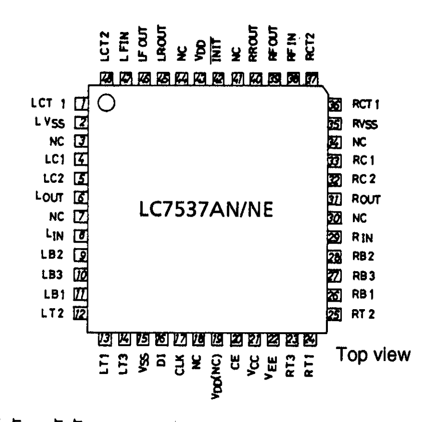
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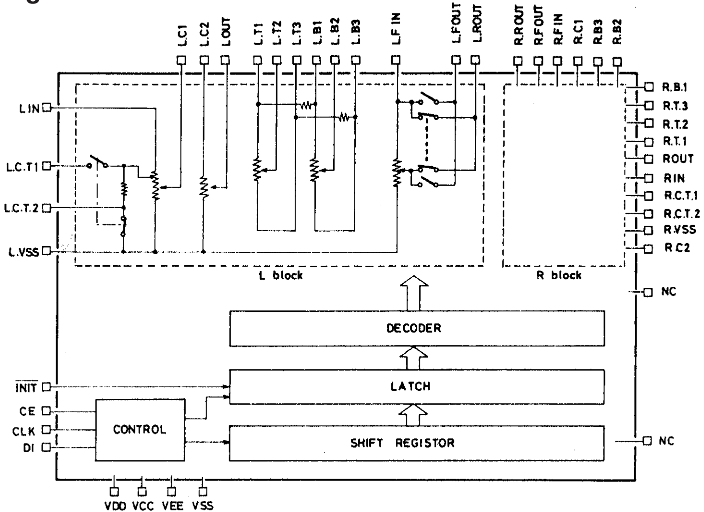


Pin Assignments





Equivalent Circuit Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V, V_{DD} = ≥ V_{CC} > V_{SS} ≥ V_{EE}

Item	Symbol	Condition	Rating	Unit
Maximum supply voltage	$V_{DD} - V_{EE}$ max	V_{DD}, V_{EE} : $V_{EE} \geq -8$ V	16	V
	V_{CC} max	V_{CC} : $V_{DD} \geq V_{CC}$	V_{SS} – 0.3 to V_{SS} + 7	V
Input supply voltage	V_{I1}	DI, CLK, CE	V_{SS} – 0.3 to V_{DD} + 0.3	V
	V_{I2}	$\overline{\text{INIT}}$	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85˚C, (LC7537N, 7537AN)	200	mW
		Ta ≤ 85˚C, (LC7537NE)	300	mW
Operating temperature	Topr		–40 to +85	˚C
Storage temperature	Tstg *3		–50 to +125	˚C

Allowable Operating Conditions at Ta = 25°C, V_{SS} = 0 V, V_{DD} = ≥ V_{CC} > V_{SS} ≥ V_{EE}

Item	Symbol	Condition	Rating	Unit
Supply voltage *1	$V_{DD} - V_{EE}$	$V_{EE} \geq -7.5$ V	4.5 to 15	V
	V_{CC}		4.5 to 5.5	V
Input high–level voltage	V_{IH1} *2	DI, CLK, CE	0.8 V_{CC} to V_{CC}	V
	V_{IH2}	$\overline{\text{INIT}}$	0.8 ($V_{DD} - V_{EE}$) + V_{EE} to V_{DD}	V
Input low–level voltage	V_{IL1} *2	DI, CLK, CE	V_{SS} to 0.2 V_{CC}	V
	V_{IL2}	$\overline{\text{INIT}}$	V_{EE} to 0.2 ($V_{DD} - V_{EE}$) + V_{EE}	V
Input signal amplitude	V_{IN}		V_{EE} to V_{DD}	$V_{P\text{-}P}$
Input pulse width	$t\o_W$		1 min	µs
setup time	$t_{set\ up}$		1 min	µs
Hold time	t_{hold}		1 min	µs
Operating frequency	f_{opg}		up to 330	kHz

Note: 1. A1000 pF or larger capacitor should be added on between each individual power supply terminal and V_{SS}.

2. When the microcomputer side control signals rise faster than V_{DD} for the LC7537, a 2 kΩ or higher resistor should be inserted midway on each of the DI, CLK, and CE lines.

3. When mounting the QIP package on the board, do not dip the entire package in solder. Only the LC7537NE may be dipped directly in solder during mounting.

Electrical Characteristics at Ta = 25°C, V_{DD} =+7.5 V, V_{EE} =–7.5 V, V_{CC} =+5 V

Item	Symbol	Condition	Rating			
			min	typ	max	Unit
Total harmonic	THD(1)	V_{IN} = 1 V, f = 1kHz, all flat overall		0.005	0.01	%
Distortion	THD(2)	V_{IN} = 1 V, f = 20 kHZ, all flat overall	0.006	0.02	%	
Crosstalk	CT	V_{IN} = 1 V, f = 1 kHz, all flat, Rg = 1 kΩ	60	95		dB
	V_{omin}(1)	V_{IN} = 1 V, f = 1 kHz, MAIN, VR = ∞, FADER VR = ∞	80	90	dB	
Maximum attenuation output	V_{omin}(2)	V_{IN} = 1 V, f = 1 kHz, MAIN, VR = ∞, V_{DD} = 8 V, FADER VR = ∞, V_{EE} = V_{SS} = 0 V, C between V_{SS} and GND of L/R = 1000 µF	70	80		dB
VR resistance voltage	R_{VOL}(1)	5 dB-step	12	20	28	kΩ
	R_{VOL}(2)	1 dB-step	12	20	28	kΩ
	R_{BASS}		12	20	28	kΩ
	R_{TREBLE}		12	20	28	kΩ
	R_{FADER}		12	20	28	kΩ
Output noise	V_N(1)	All flat overall (I_{HF-A}) Rg = 1 kΩ		2	10	µV
	V_N(2)	Rg = 1 kΩ, V_{DD} = 8 V, V_{EE} = V_{SS} = 0 V		2	10	µV
Current drain	I_{DD}	V_{DD} – V_{EE} = 15 V			1	mA
	I_{CC}	V_{CC} = 5 V			1	mA

Pin Description ( ) : LC7537AN, 7537NE

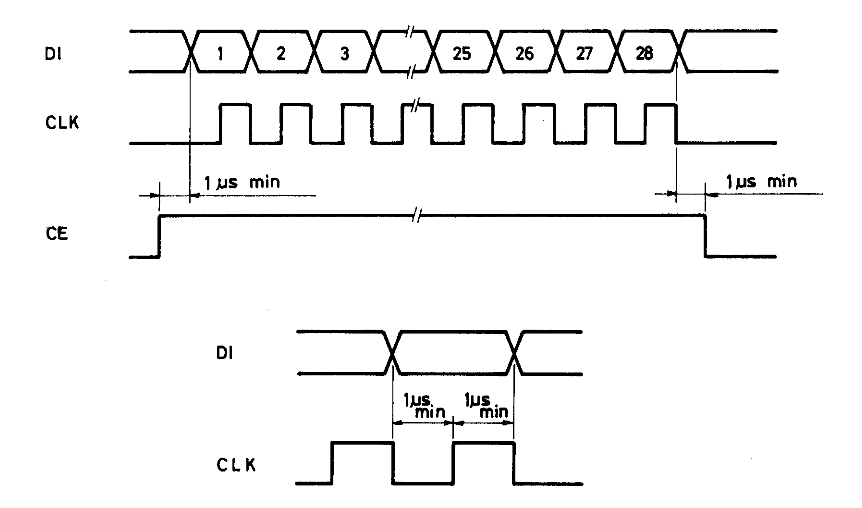
Pin No.	Symbol	Description of Functions	Remarks
12(8)	L.IN	Main volume control block 5 dB-step attenuator input terminals. These pins should be driven at a low impedance.	
31(29)	R.IN		
9(4)	L.C1	Main volume control block 5 dB-step attenuator output terminals. Having been designed to be open, the step positions will develop errors if at low acceptor impedances, so that as high load impedances as possible should be provided.	VR resistance : 20 kΩ
34(33)	R.C1		
10(5)	L.C2	Main volume control block 1 dB-step attenuator input terminals. Theses pins should be driven at alow impedance.	
33(32)	R.C2		
11(6)	L.OUT	Main volume control block 1 dB-step attenuator output terminals. Due to the step positions designed to be open, load impedances as high as possible should be provided to them, similar to those for the LC1 and RC1.	VR resistance : 20 kΩ
32(31)	R.OUT		
5(47)	L.FIN	Fader functions employing mode input terminals. These pins should be driven at a low impedance.	
38(38)	R.FIN		
4(46)	L.FOUT	Fader block output terminals. These pins permit the front and rear sides to be faded out independently of each other. Attenuations exercised on Lch will be the same as on Rch. Due to the step positions designed to be open, acceptor impedances as high as possible should be provided to them.	VR resistance : 20 kΩ
3(45)	L.ROUT		
39(39)	R.ROUT		
40(40)	R.ROUT		
15(11)	L.B1	Bass tone control block terminals. A total of 15 positions have been provided in 2 dB steps	VR resistance : 20 kΩ
16(9)	L.B2		
14(10)	L.B3		
28(26)	R.B1		
27(28)	R.B2		
29(27)	R.B3		
17(13)	L.T1	Treble tone control block terminals. A total of 15 positions have been provided in 2 dB steps. The VR resistance value is 20 kΩ.	VR resistance : 20 kΩ
16(12)	L.T2		
18(14)	L.T3		
26(24)	R.T1		
27(25)	R.T2		
25(23)	R.T3		
7(1)	LCT1	Loudness dedicated terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range correcting C between CT2 and L–V_{SS} (R–V_{SS}).	
6(48)	LCT2		
36(36)	RCT1		
37(37)	RCT2		

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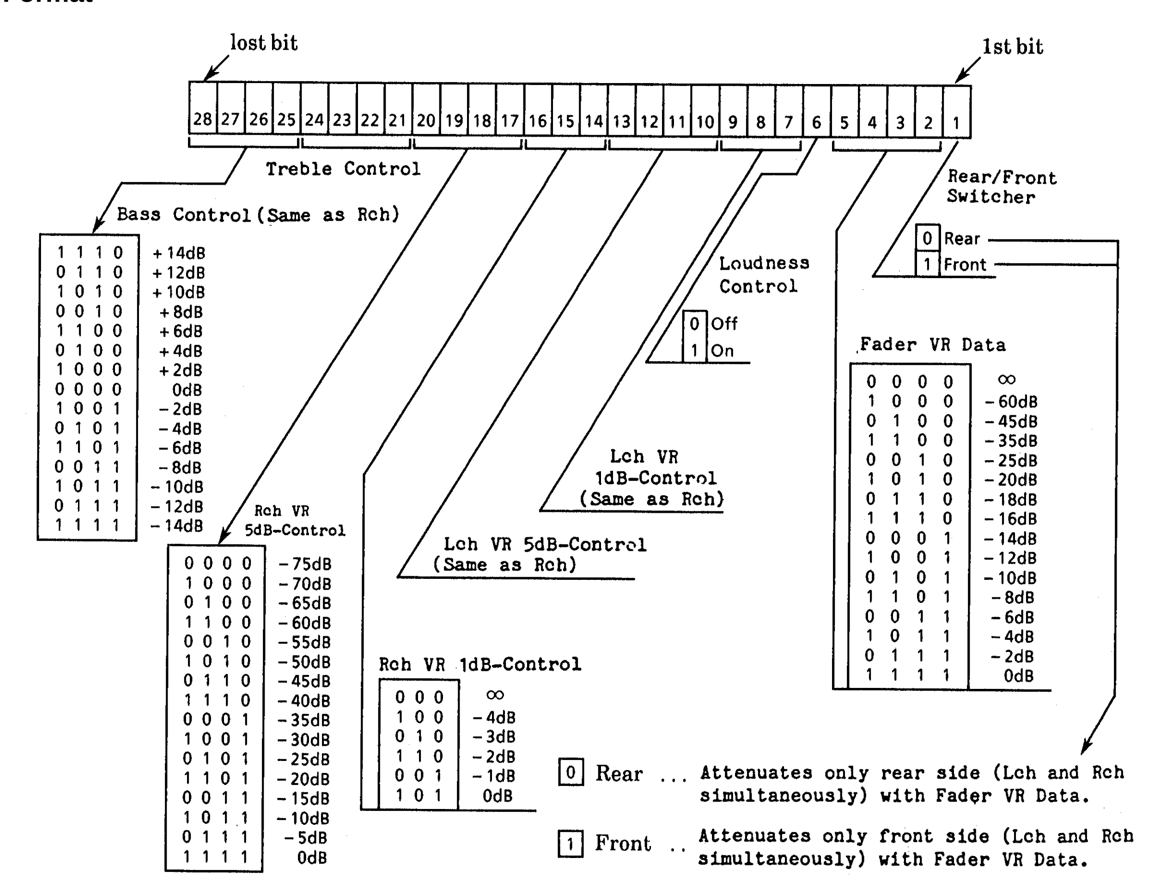
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Pin No.	Symbol	Description of Functions	Remarks
8(2)	L-V_{SS}	Main volume control block fader control common terminals. The impedance of pattern connected to these pins should be as low as possible. Since L–V_{SS} (R–V_{SS}) and V_{SS} have not been connected inside the LSI, they should be connected together on the outside in conformance with their individual specifications. Particular attenuation should be paid to the capacitance assigned to the capacitors put between L–V_{SS} (R–V_{SS}) and V_{SS}, which will emerge as a residual resistive component when control is turned down for maximum attenuation.	
35(35)	R-V_{SS}		
42(42)	$\overline{\text{INIT}}$	Intra-IC latch resetting terminal Control-setting data at the internal latch will be indeterminate when power has just been switched on, so that by engaging the "L" level of this pin at power-on, the fader control may be set at its –∞ position and muting behaviour is engaged (Note: V_{DD} to V_{EE} Level).	
22(20)	CE	Chip enable terminal. When this pin is made "H" to "L", data is written in the internal latch, activating the various analog switches. When the "H" level is then restored, transfer of the data will be enabled.	
20(16)	DI	Input terminals for serial data and clock that serve control purposes.	
21(17)	CLK		
1(43) 23(21) 19(15) 24(22)	V_{DD} V_{CC} V_{SS} V_{EE}	These pins are connected to the relevant power supplies. Exercise caution against V_{CC} rising earlier than V_{DD}.	
2(3, 7) 41(18, 30, 34, 41, 44)	NC	No connect pins. Absolutely nothing should be connected here.	
(19)	V_{DD}(NC)	V_{DD} subterminal. Connected to V_{DD} or left open.	LC7537AN and LC7537NE only

Control Timing



Data Format



Bass Control (Same as Rch)

1 1 1 0	+14dB
0 1 1 0	+12dB
1 0 1 0	+10dB
0 0 1 0	+8dB
1 1 0 0	+6dB
0 1 0 0	+4dB
1 0 0 0	+2dB
0 0 0 0	0dB
1 0 0 1	−2dB
0 1 0 1	−4dB
1 1 0 1	−6dB
0 0 1 1	−8dB
1 0 1 1	−10dB
0 1 1 1	−12dB
1 1 1 1	−14dB

Rch VR 5dB-Control

0 0 0 0	−75dB
1 0 0 0	−70dB
0 1 0 0	−65dB
1 1 0 0	−60dB
0 0 1 0	−55dB
1 0 1 0	−50dB
0 1 1 0	−45dB
1 1 1 0	−40dB
0 0 0 1	−35dB
1 0 0 1	−30dB
0 1 0 1	−25dB
1 1 0 1	−20dB
0 0 1 1	−15dB
1 0 1 1	−10dB
0 1 1 1	−5dB
1 1 1 1	0dB

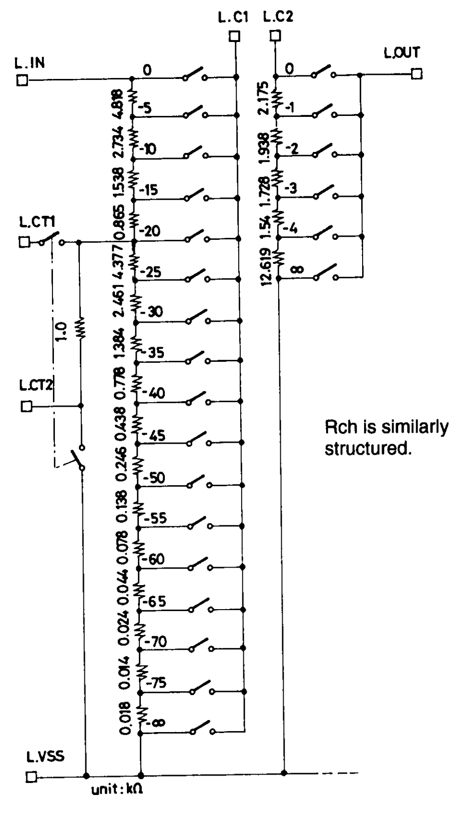
Rch VR 1dB-Control

0 0 0	∞
1 0 0	−4dB
0 1 0	−3dB
1 1 0	−2dB
0 0 1	−1dB
1 0 1	0dB

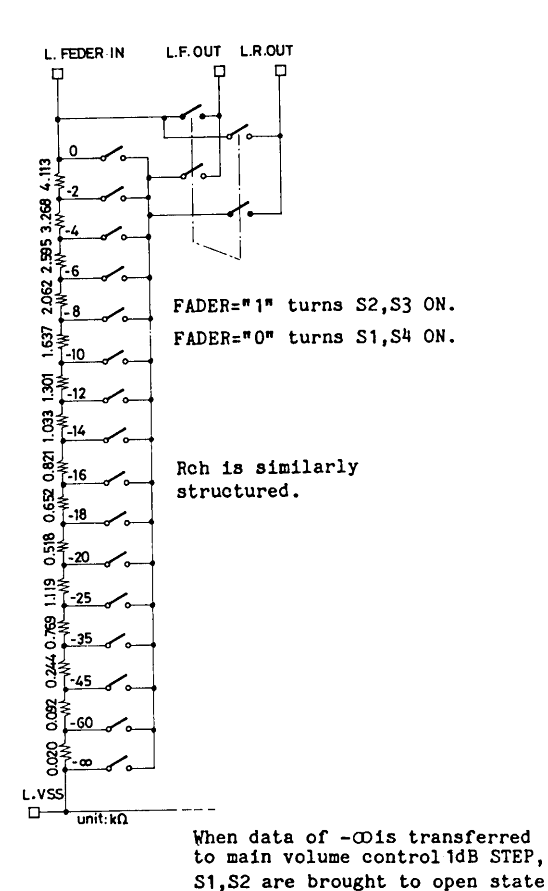
Fader VR Data

0 0 0 0	∞
1 0 0 0	−60dB
0 1 0 0	−45dB
1 1 0 0	−35dB
0 0 1 0	−25dB
1 0 1 0	−20dB
0 1 1 0	−18dB
1 1 1 0	−16dB
0 0 0 1	−14dB
1 0 0 1	−12dB
0 1 0 1	−10dB
1 1 0 1	−8dB
0 0 1 1	−6dB
1 0 1 1	−4dB
0 1 1 1	−2dB
1 1 1 1	0dB

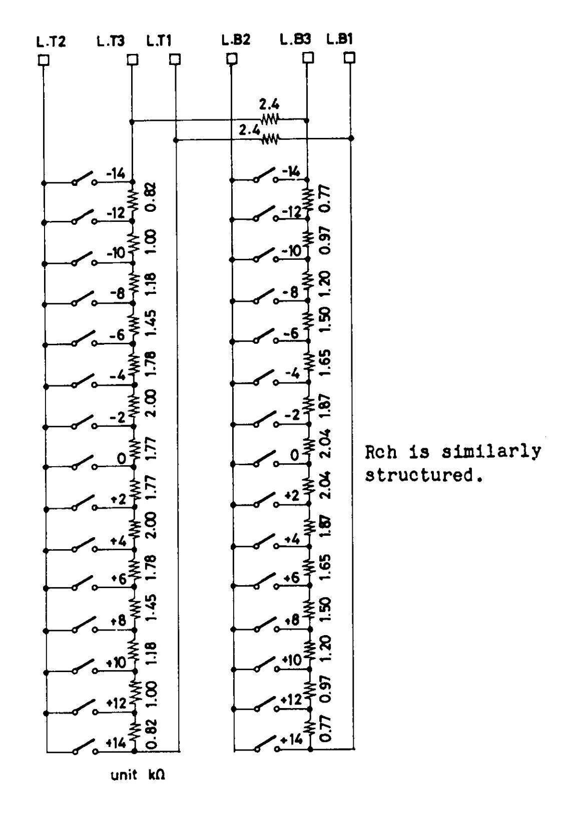
Main Volume Control Block Equivalent Circuit



Fader Volume Control Block Equivalent Circuit

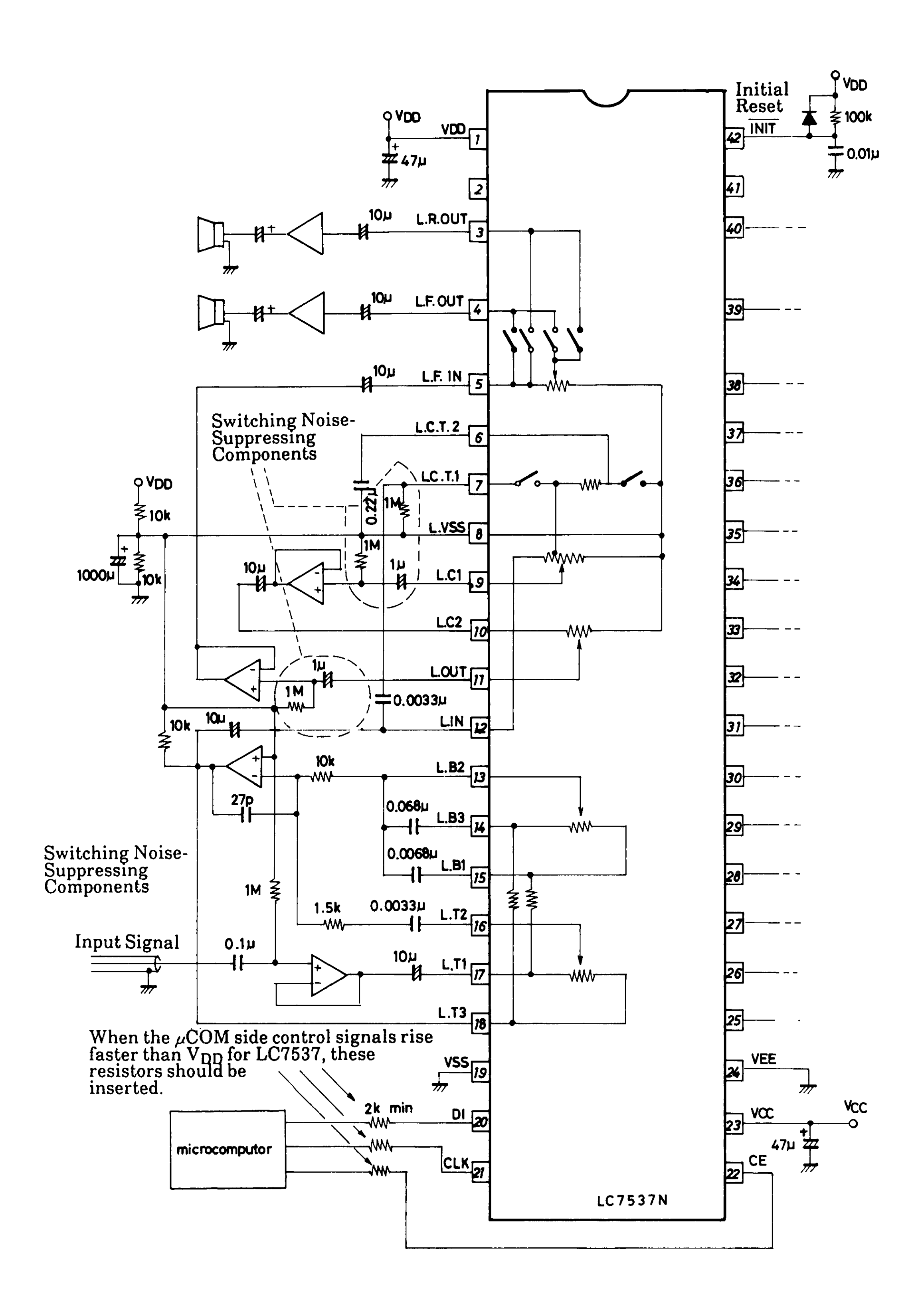


Tone Control Block Equivalent Circuit



Sample Application Circuits

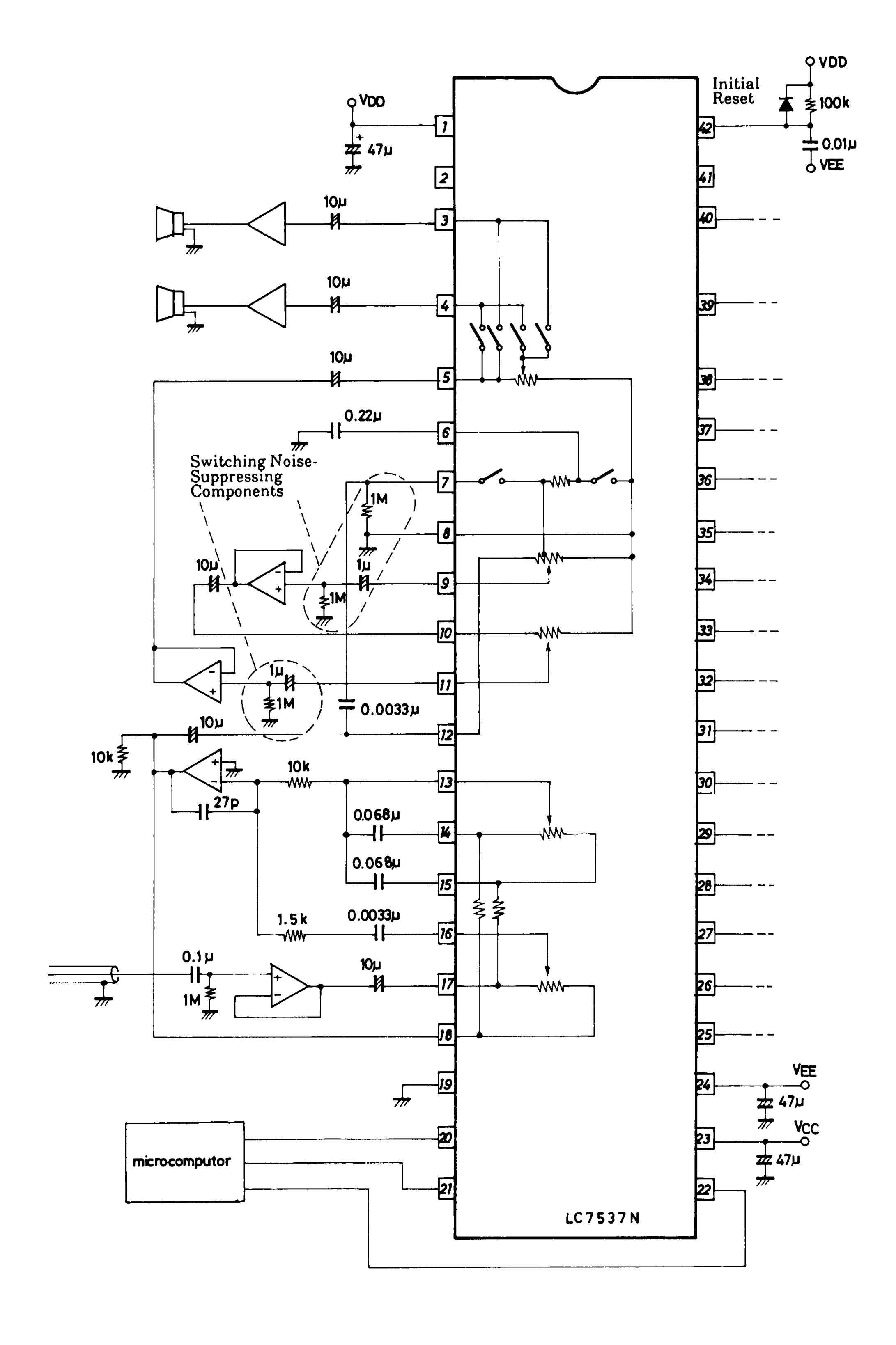
Single Power Supply



Unit (resistance: Ω, capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

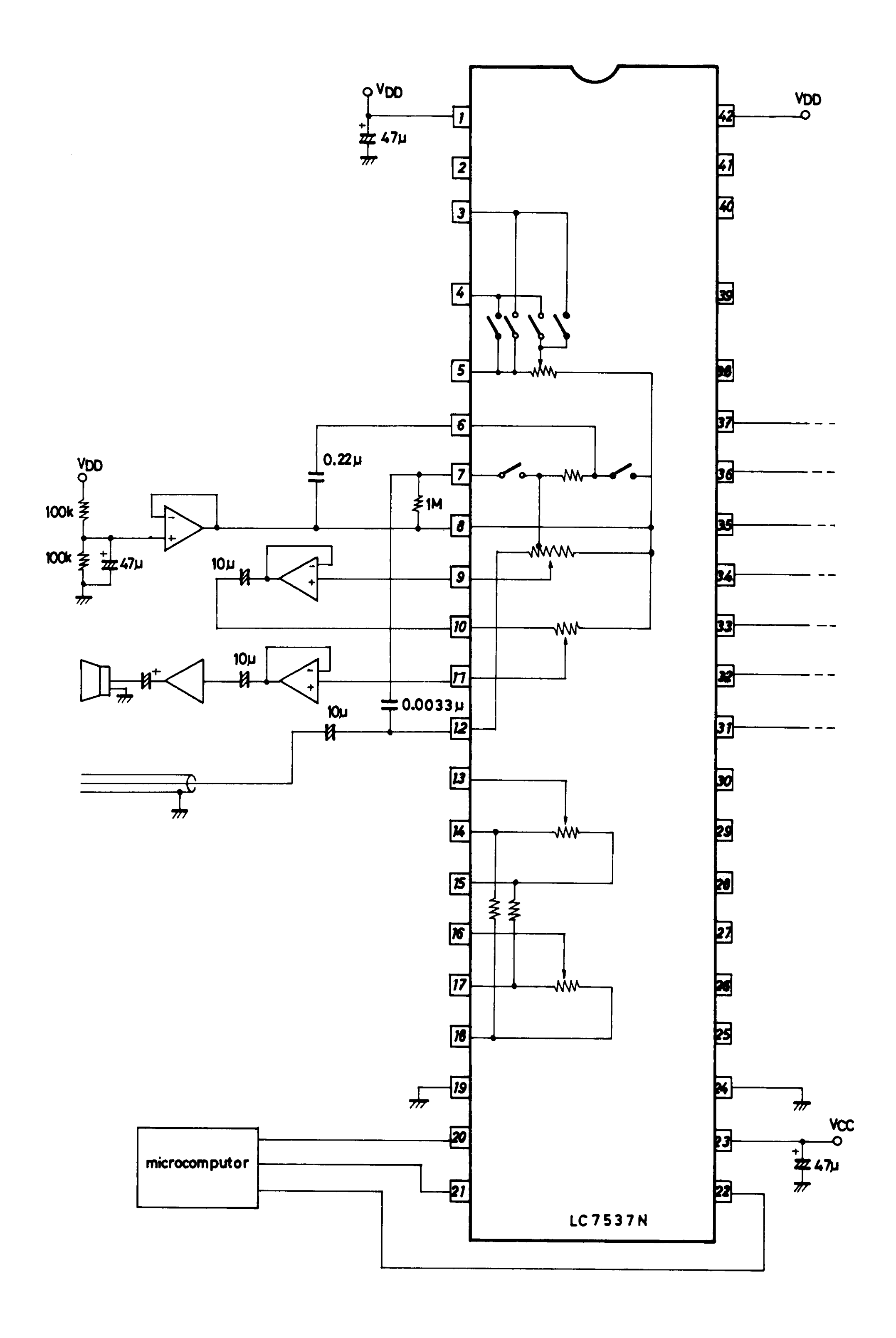
Dual ± Power Supply



Unit (resistance: Ω, capacitance: F)

Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

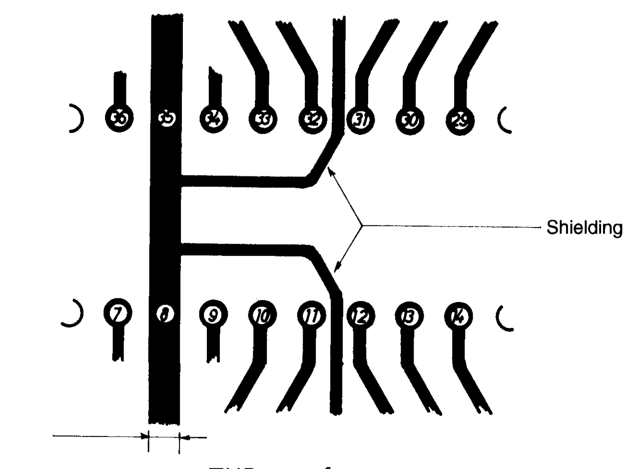
Single Power Supply



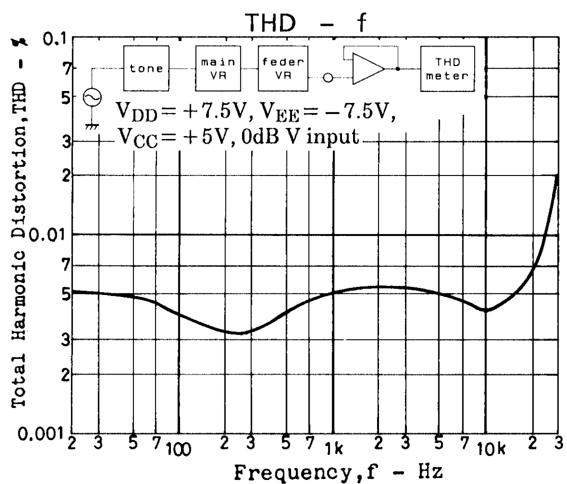
Unit (resistance: Ω, capacitance: F)

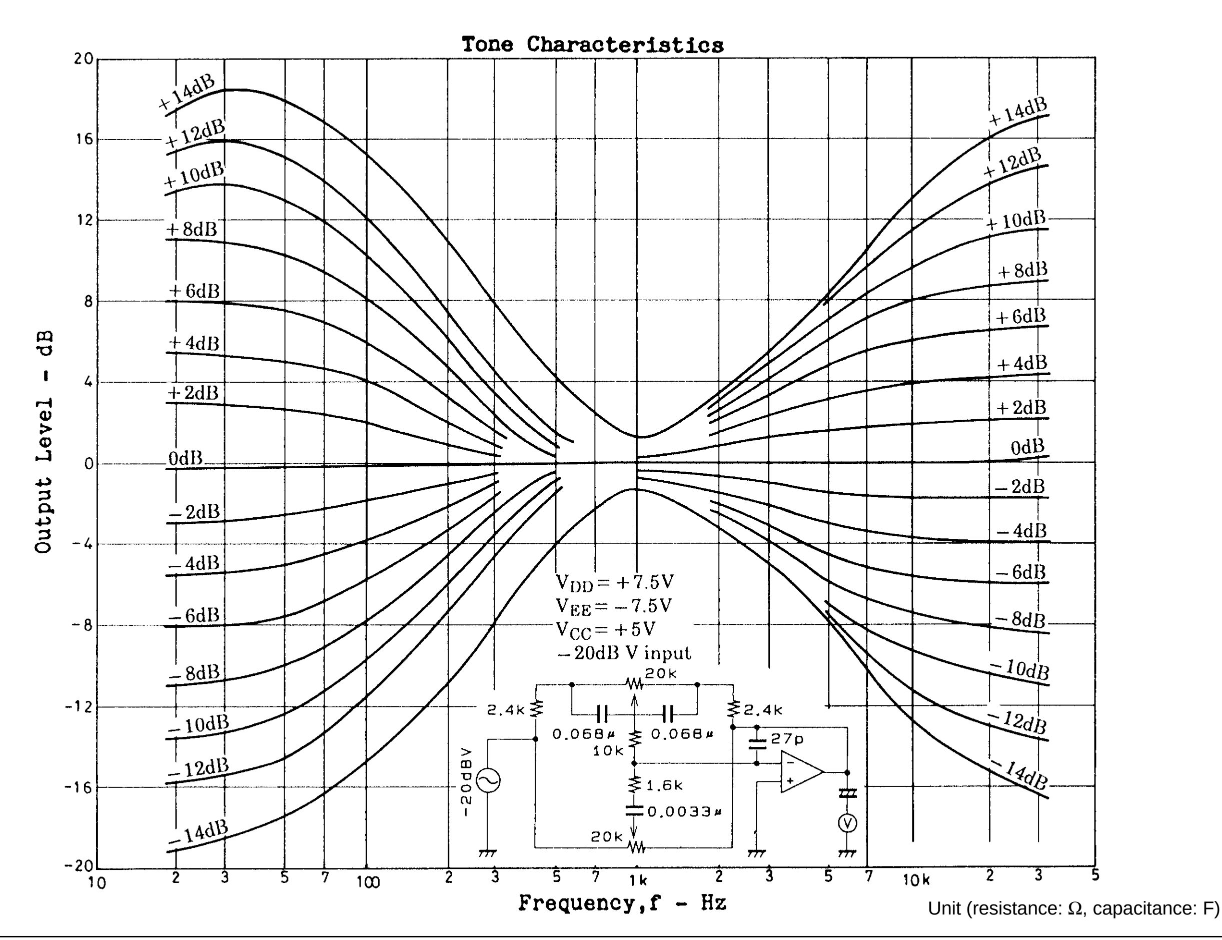
Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

Caution for Pattern Designing

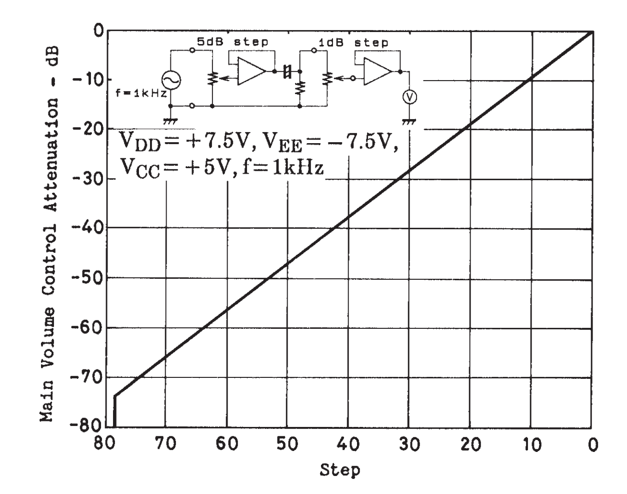


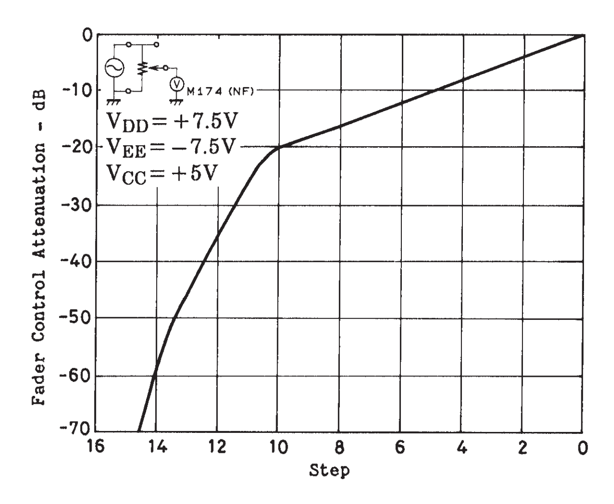
- Space the patterns between L.IN and L.OUT and those between R.IN and R.OUT as far apart as possible. When forced to design them close together, provide shielding patterns between as illustrated. They will be effective at the maximum attenuated level (with 10 kHz and higher frequencies). (DIP42S)
- Make the L–V_{SS} and R–V_{SS} as broad as possible.





Unit (resistance: Ω, capacitance: F)





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